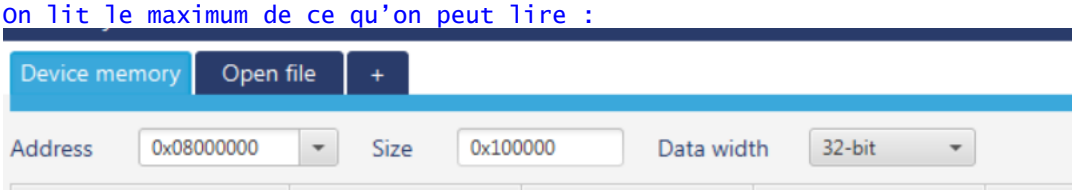
1) On vérifie qu'on a le bon câble USB !!! Important car la première fois j'ai passé 2 heures à chercher pourquoi je n'arrivais pas à connecter STM32CubeProgrammer à la carte NUCLEA-H755ZI-Q… Mon câble semblait correct mais ne contenait que les connexion d'alimentation !
2) On regarde ce qui est indiqué ici et l'on voit que la carte est détectée, le port SWD en mode normal à la fréquence de 24000 nous convient>…

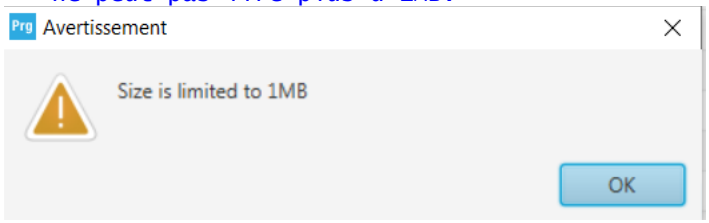
3) Nous n'avons plus qu'à cliquer sur le bouton Connect

```
15:23:50 : ST-LINK SN : 004700433038510234333935
15:23:50 : ST-LINK FW : V3J2M1
15:23:50 : Voltage : 3.30V
15:23:50 : SWD freq : 24000 KHz
15:23:50 : Connect mode: Normal
15:23:50 : Reset mode : Software reset
15:23:50 : Device ID : 0x450
15:23:51 : UPLOADING OPTION BYTES DATA ...
15:23:51 : Bank : 0x00
15:23:51 : Address : 0x5200201c
15:23:51 : Size : 308 Bytes
15:23:51 : UPLOADING ...
15:23:51 : Size : 1024 Bytes
15:23:51 : Address : 0x8000000
15:23:51 : Read progress:
15:23:51 : Data read successfully
15:23:51 : Time elapsed during the read operation is: 00:00:00.002
```

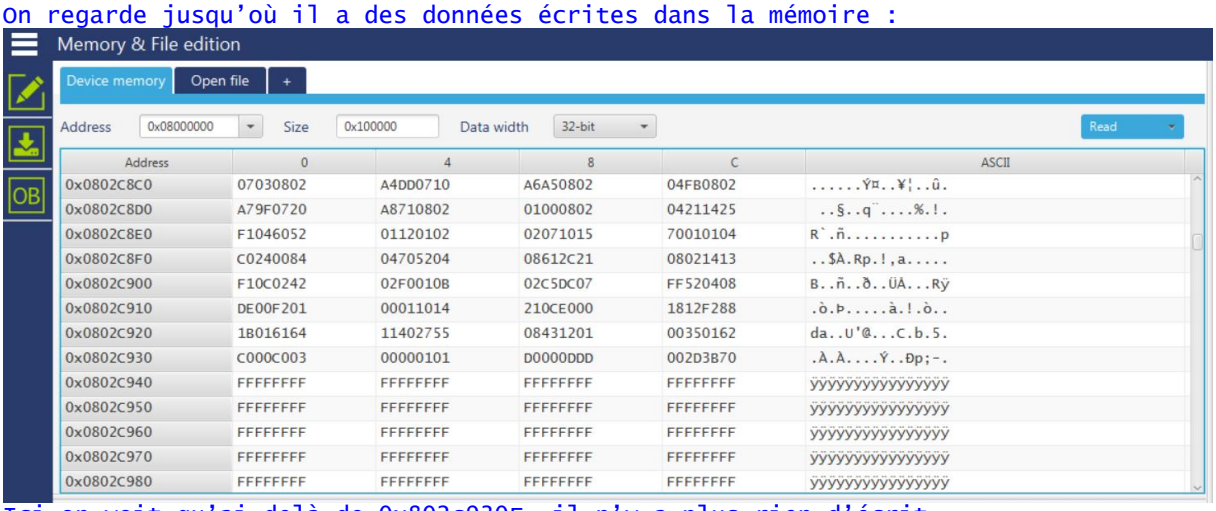
4) On lit le maximum de ce qu'on peut lire :



5) Si l'on met plus que 0x100000, On obtient un message d'erreur indiquant qu'on ne peut pas lire plus d'1MB.

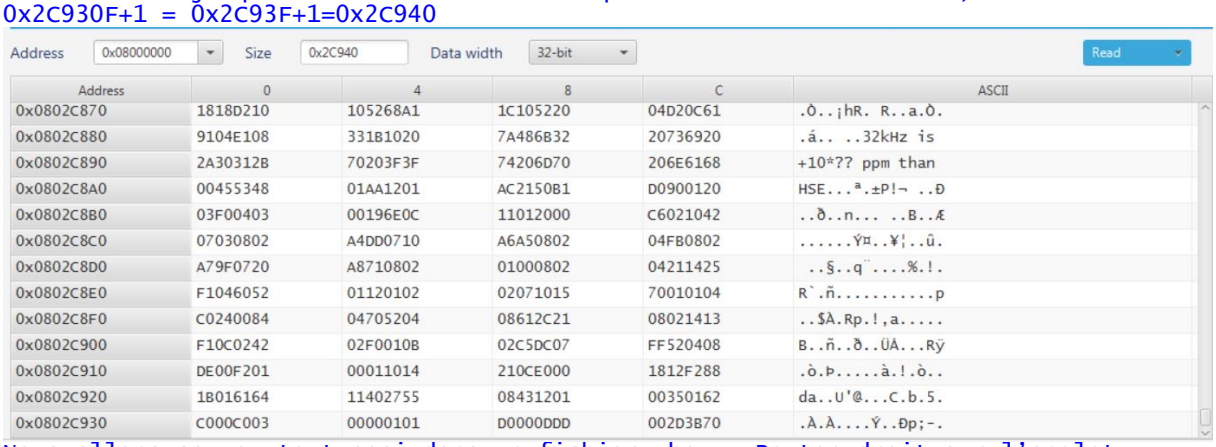


6) On regarde jusqu'où il a des données écrites dans la mémoire :



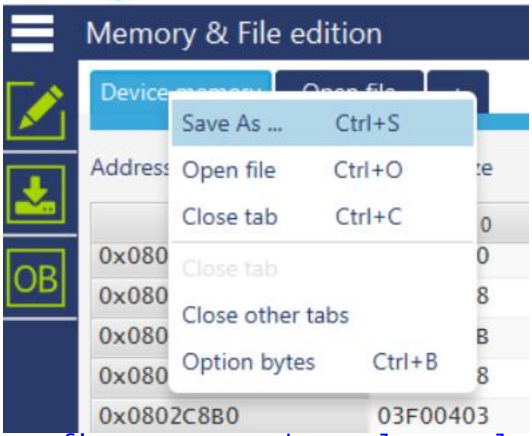
Address	0	4	8	C	ASCII
0x0802C8C0	07030802	A4DD0710	A6A50802	04FB0802	......ý¤..¥¦..û.
0x0802C8D0	A79F0720	A8710802	01000802	04211425	..§..q¨....%.!.
0x0802C8E0	F1046052	01120102	02071015	70010104	R`.ñ..........p
0x0802C8F0	C0240084	04705204	08612C21	08021413	..$À.Rp.!,a.....
0x0802C900	F10C0242	02F0010B	02C5DC07	FF520408	B..ñ..ð..ÜÅ...Rÿ
0x0802C910	DE00F201	00011014	210CE000	1812F288	.ò.Þ.....à.!.ò..
0x0802C920	1B016164	11402755	08431201	00350162	da..U'@...C.b.5.
0x0802C930	C000C003	00000101	D0000DDD	002D3B70	.À.À....Ý..Ðp;-.
0x0802C940	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0x0802C950	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0x0802C960	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0x0802C970	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0x0802C980	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ

7) Ici on voit qu'ai delà de 0x802c930F, il n'y a plus rien d'écrit.
8) On va relire jusqu'à cette limite en indiquant la taille souhaitée, ici 0x2C930F+1 = 0x2C93F+1=0x2C940

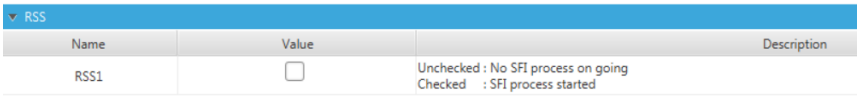


Address	0	4	8	C	ASCII
0x0802C870	1818D210	105268A1	1C105220	04D20C61	.Ò..¡hR. R..a.Ò.
0x0802C880	9104E108	331B1020	7A486B32	20736920	.á.. ..32kHz is
0x0802C890	2A30312B	70203F3F	74206D70	206E6168	+10*?? ppm than
0x0802C8A0	00455348	01AA1201	AC2150B1	D0900120	HSE...ª.±P!¬ ..Ð
0x0802C8B0	03F00403	00196E0C	11012000	C6021042	..ð..n... ..B..Æ
0x0802C8C0	07030802	A4DD0710	A6A50802	04FB0802	......ý¤..¥¦..û.
0x0802C8D0	A79F0720	A8710802	01000802	04211425	..§..q¨....%.!.
0x0802C8E0	F1046052	01120102	02071015	70010104	R`.ñ..........p
0x0802C8F0	C0240084	04705204	08612C21	08021413	..$À.Rp.!,a.....
0x0802C900	F10C0242	02F0010B	02C5DC07	FF520408	B..ñ..ð..ÜÅ...Rÿ
0x0802C910	DE00F201	00011014	210CE000	1812F288	.ò.Þ.....à.!.ò..
0x0802C920	1B016164	11402755	08431201	00350162	da..U'@...C.b.5.
0x0802C930	C000C003	00000101	D0000DDD	002D3B70	.À.À....Ý..Ðp;-.

9) Nous allons sauvez tout ceci dans un fichier .hex : Bouton droit sur l'onglet « Device memory » puis « Save As » puis l'on choisit un endroit et un nom de fichier ad'hoc



10) Maintenant, on en profite pour regarder quels sont les paramètres en cliquant sur le bouton « OB » = Option Byte



BOR Level

Name	Value	Description
BOR_LEV	0	These bits reflects the power level that generates a system reset Refer to device datasheet for the values of VBORx VDD reset thresholds. 0 : reset level is set to VBOR0 1 : reset level is set to VBOR1 2 : reset level is set to VBOR2 3 : reset level is set to VBOR3

User Configuration

Name	Value	Description
IWDG1_SW	☑	Unchecked : Independent watchdog is controlled by hardware Checked : Independent watchdog is controlled by software
IWDG2_SW	☑	Unchecked : Independent watchdog is controlled by hardware Checked : Independent watchdog is controlled by software
NRST_STOP_D1	☑	Unchecked : STOP mode on Domain 1 is entering with reset Checked : STOP mode on Domain 1 is entering without reset
NRST_STBY_D1	☑	Unchecked : STANDBY mode on Domain 1 is entering with reset Checked : STANDBY mode on Domain 1 is entering without reset
FZ_IWDG_STOP	☑	Unchecked : Independent watchdog is freezed in STOP mode Checked : Independent watchdog is running in STOP mode
FZ_IWDG_SDBY	☑	Unchecked : Independent watchdog is freezed in STANDBY mode Checked : Independent watchdog is running in STANDBY mode
SECURITY	☐	Unchecked : Security feature disabled Checked : Security feature enabled
BCM4	☑	Unchecked : CM4 boot disabled Checked : CM4 boot enabled
BCM7	☑	Unchecked : CM7 boot disabled Checked : CM7 boot enabled
NRST_STOP_D2	☑	Unchecked : STOP mode on Domain 2 is entering with reset Checked : STOP mode on Domain 2 is entering without reset
NRST_STBY_D2	☑	Unchecked : STANDBY mode on Domain 2 is entering with reset Checked : STANDBY mode on Domain 2 is entering without reset
SWAP_BANK	☐	Unchecked : after boot loading, no swap for user sectors Checked : after boot loading, user sectors swapped

Boot address Option Bytes

Name	Value	Description
BOOT_CM7_ADD0	Value 0x800 Address 0x8000000	Define the boot address for Cortex-M7 when BOOT0=0
BOOT_CM7_ADD1	Value 0x1ff0 Address 0x1ff00000	Define the boot address for Cortex-M7 when BOOT0=1
BOOT_CM4_ADD0	Value 0x810 Address 0x8100000	Define the boot address for Cortex-M4 when BOOT0=0
BOOT_CM4_ADD1	Value 0x1000 Address 0x10000000	Define the boot address for Cortex-M4 when BOOT0=1

PCROP Protection

Name	Value	Description
PROT_AREA_START1	Value 0xff Address 0x800ff00	Flash Bank 1 PCROP start address
PROT_AREA_END1	Value 0x0 Address 0x80000ff	Flash Bank 1 PCROP End address (excluded) Deactivation of PCROP can be done by enbaling DMEP1 bit and changing RDP from level 1 to level 0 while puttin
DMEP1	☐	Unchecked : Flash Bank 1 PCROP zone is kept when RDP level regression (change from level 1 to 0) occurs Checked : Flash Bank 1 PCROP zone is erased when RDP level regression (change from level 1 to 0) occurs
PROT_AREA_START2	Value 0xff Address 0x810ff00	Flash Bank 2 PCROP start address
PROT_AREA_END2	Value 0x0 Address 0x81000ff	Flash Bank 2 PCROP End address Deactivation of PCROP can be done by enbaling DMEP2 bit and changing RDP from level 1 to level 0 while puttin
DMEP2	☐	Unchecked : Flash Bank 2 PCROP zone is kept when RDP level regression (change from level 1 to 0) occurs Checked : Flash Bank 2 PCROP zone is erased when RDP level regression (change from level 1 to 0) occurs

Secure Protection

Name	Value	Description
SEC_AREA_START1	Value 0xff Address 0x800ff00	Flash Bank 1 secure area start address
SEC_AREA_END1	Value 0x0 Address 0x80000ff	Flash Bank 1 secure area end address If this address is equal to SEC_AREA_START1, the whole bank 1 is secure protected.If this address is lower than SE
DMES1	☐	Unchecked : Flash Bank 1 secure area is kept when RDP level regression (change from level 1 to 0) occurs Checked : Flash Bank 1 secure area is erased when RDP level regression (change from level 1 to 0) occurs
SEC_AREA_START2	Value 0xff Address 0x810ff00	Flash Bank 2 secure area start address
SEC_AREA_END2	Value 0x0 Address 0x81000ff	Flash Bank 2 secure area end address If this address is equal to SEC_AREA_START2, the whole bank 2 is secure protected.If this address is lower than SE
DMES2	☐	Unchecked : Flash Bank 2 secure area is kept when RDP level regression (change from level 1 to 0) occurs Checked : Flash Bank 2 secure area is erased when RDP level regression (change from level 1 to 0) occurs

DTCM RAM Protection

Name	Value	Description
ST_RAM_SIZE	0	0 : 2 KB 1 : 4 KB 2 : 8 KB 3 : 16 KB

Protection

Name	Value	D
nWRP0	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP1	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP2	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP3	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP4	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP5	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP6	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP7	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP8	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP9	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP10	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP11	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP12	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP13	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP14	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector
nWRP15	☑	Unchecked : Write protection active on this sector Checked : Write protection not active on this sector